ABSTRACT OF THE DISCLOSURE

A system LSI is provided which has a function of enabling data of an external device to be correctly read, when high-speed testing is carried out at a clock signal which is higher-speed than that at a time of usual operation. The system LSI has an external terminal for input of a wait signal from a testing device which is connected when high-speed testing is carried out. Moreover, when the wait signal is supplied to an external bus controller, the external bus controller extends an access time to a ROM during a period of time over which the wait signal is supplied.